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☐ 1. Document ID: US 20040075653 A1

Using default format because multiple data bases are involved.

L8: Entry 1 of 15 File: PGPB Apr 22, 2004

PGPUB-DOCUMENT-NUMBER: 20040075653
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040075653 A1

TITLE: Continuous graphics display for single display device during the processor non-responding period

PUBLICATION-DATE: April 22, 2004

INVENTOR-INFORMATION:

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US-CL-CURRENT: 345/204

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Ds

☐ 2. Document ID: US 20040044710 A1

L8: Entry 2 of 15 File: PGPB Mar 4, 2004

DOCUMENT-IDENTIFIER: US 20040044710 A1
TITLE: Converting mathematical functions to power series

Detail Description Paragraph:
[0015] Referring to FIG. 1, in one embodiment, a system 10 includes processor 100, which may be a general-purpose or special-purpose processor such as a microprocessor, microcontroller, an application-specific integrated circuit (ASIC), a programmable gate array (PGA), and the like. The processor 100 may be coupled over a host bus 103 to a memory hub 108 in one embodiment, which may include a memory controller 107 coupled to a main memory 106. In addition, the memory hub 108 may include cache controller 105 coupled to an L2 cache 104. The memory hub 108 may also include a graphics interface 111 that is coupled over a link 109 to a graphics

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controller 110, which in turn may be coupled to a display 112. As an example, the graphics interface 111 may conform to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, dated in May 1998.

☐ 3. Document ID: US 20040025083 A1

L8: Entry 3 of 15 File: PGPB Feb 5, 2004

DOCUMENT-IDENTIFIER: US 20040025083 A1
TITLE: Generating test code for software

Detail Description Paragraph:
[0032] Now referring to FIG. 4, in one embodiment, a system 10 includes a processor 100, which may include a general-purpose or special-purpose processor such as a microprocessor, microcontroller, an application-specific integrated circuit (ASIC), a programmable gate array (PGA), and the like. The processor 100 may be coupled over a host bus 103 to a memory hub 108 in one embodiment, which may include a memory controller 107 coupled to a main memory 106. In addition, the memory hub 108 may include cache controller 105 coupled to an L2 cache 104. The memory hub 108 may also include a graphics interface 111 that is coupled over a link 109 to a graphics controller 110, which may be coupled to a display 112. As an example, the graphics interface 111 may conform to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, dated in May 1998.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20040010464 A1

L8: Entry 4 of 15 File: PGPB Jan 15, 2004

DOCUMENT-IDENTIFIER: US 20040010464 A1
TITLE: Communication device and method for implementing communication on a wide area network

Detail Description Paragraph:
[0033] Processor 204 connects to front side system bus 205, which allows processor 204 to communicate with main memory 207 (usually random access memory (RAM)), chipset 210, and L2 cache 206. Ideally, processor 204 is specifically designed for multimedia data transfer such as a 1.8 GHz Intel.RTM. Pentium 4 processor which uses a 400 MHz system bus (front side bus 205) and is available from Intel Corporation in Santa Clara, Calif. which uses a 400 MHz system bus (front side bus 205). Bridge 210 may also include an integrated memory controller and cache memory for processor 204. Additional connections to any of the buses depicted may be made through direct component interconnection or through add-in boards. In the depicted example, AGP bus 220 provides a communications link between processor 204, memory 207 and video/graphics card 222 which, in turn, supports any one of a variety of types of monitors 224. A conventional video monitor may be used for practicing the

present invention or in accordance with other embodiments; a touch screen display is used for both displaying video images and receiving user interaction input. Also needed for the present invention is a means for capturing real-time video images such as video camera 266 which is shown connected to USB bus 230 through multi-port USB hub 232. Video camera 266 is often referred to as a net- or web-camera (shortened to webcam or netcam) because it is specifically designed to be used with network applications. It should be understood that, while the present example depicts video camera 266 as a USB type camera, the USB bus is considered to have a relatively low data transfer rate. Low data transfer rates lessen the amount of video pixel data that can be transferred for a given time period. Low data transfer rates are normally accommodated in one of four ways: smaller image frame; lower image frame rate; lower image resolution; and lower color resolution. These techniques can be used independently, or several techniques may be combined to accommodate narrower bandwidth constraints. However, each of these methods detracts from the user's overall enjoyment and appreciation of the image, and therefore, they should be used sparingly or avoided if adequate bandwidth permits. Therefore, while in the present example video camera 266 is depicted as a USP camera, others types of video cameras are known which generally achieve higher data transfer rates. These may be connected to either Industry Standard Architecture (ISA) bus 250 or Perpipheral Component Interconnect (PCI) bus 240. ISA bus 250 is generally used for slower devices, while PCI bus 240 connects the fast devices to the CPU. ISA is an older, lower capacity type of bus and may not be present in all data processing systems. Thus, PC bus 240 is the logical choice for higher data transfer rates. Below is a table listing the data transfer attributes for several popular types of local bus architectures.

☐ 5. Document ID: US 20030070014 A1

L8: Entry 5 of 15 File: PGPB Apr 10, 2003

DOCUMENT-IDENTIFIER: US 20030070014 A1
TITLE: Data transfer in host expansion bridge

Detail Description Paragraph:
[0025] Attention now is directed to FIG. 3, an example computer system platform having an example virtual interface expansion bridge (VXB) incorporated therein according to the principles of the present invention. As shown in FIG. 3, the computer system 300 may comprise a processor subsystem 310 (which may be comprised of a plurality of processors 311a-311n and at least one cache memory 312), a memory controller hub (MCH) 320 connected to the processor subsystem 310 (such as by a host interface or a front side bus), a graphics subsystem 330 (possibly including a AGP 4.times. graphics controller, a local memory and a display device such as a cathode ray tube, liquid crystal display, or flat panel display) connected to the memory controller hub 320 by a graphics bus 335 (such as an AGP 2.0 bus), and a memory subsystem 340 storing information and instructions for use by the processor subsystem 310 and having at least one memory element 342 connected to MCH 320 by a memory bus 325. The memory subsystem 340 is preferably a dynamic random-access-memory (DRAM), but may be substituted for read-only-memory (ROM), video random-access-memory (VRAM) and the like. The memory subsystem 340 stores information and instructions for use by the host processors 311a-311n.

☐ 6. Document ID: US 20020174284 A1

L8: Entry 6 of 15 File: PGPB Nov 21, 2002

DOCUMENT-IDENTIFIER: US 20020174284 A1
TITLE: Device for spatially and temporally reordering for data between a processor, memory and peripherals

Detail Description Paragraph:
[0014] FIG. 1 illustrates an example of an embodiment of the present invention in which a baseboard (mother board) 100 may contain a socket for a processor with cache memory 110 and a chipset 120. Within the chipset 120 may be contained a memory controller hub (MCH) 130 and an Input/Output (I/O) controller hub (ICH) 140. The MCH 130 may be used to control access to main memory 150 which may comprises dynamic random access memory (DRAM). The MCH 130 may also control access to an accelerated graphics port (AGP) 160 as well as other comparable devices. The MCH communicates to the processor 110 through the front side bus (FSB) 125. As will be discussed in further detail in reference to table 1 ahead, data is transferred from main memory and peripheral devices through MCH 130 to processor 110 over FSB 125 in two chunks of data where each chunk contains 256 bits of data.

☐ 7. Document ID: US 20020046325 A1

L8: Entry 7 of 15 File: PGPB Apr 18, 2002

DOCUMENT-IDENTIFIER: US 20020046325 A1
TITLE: Buffer memory management in a system having multiple execution entities

Detail Description Paragraph:
[0040] The main memory 206 is controlled by a memory controller 207 in a memory hub 208 coupled to the CPU 200 over the host bus 203. In addition, the memory hub 208 may include a cache controller 205 operatively coupled to the L2 cache 204. The memory hub 208 may also include a graphics interface 211 that is coupled over a link 209 to a graphics controller 210, which is in turn coupled to a display 212. As an example, the graphics interface may be according to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, published in May 1998.

☐ 8. Document ID: US 20010049770 A1

L8: Entry 8 of 15 File: PGPB Dec 6, 2001

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DOCUMENT-IDENTIFIER: US 20010049770 A1
TITLE: BUFFER MEMORY MANAGEMENT IN A SYSTEM HAVING MULTIPLE EXECUTION ENTITIES

Detail Description Paragraph:
[0039] The main memory 206 is controlled by a memory controller 207 in a memory hub 208 coupled to the CPU 200 over the host bus 203. In addition, the memory hub 208 may include a cache controller 205 operatively coupled to the L2 cache 204. The memory hub 208 may also include a graphics interface 211 that is coupled over a link 209 to a graphics controller 210, which is in turn coupled to a display 212. As an example, the graphics interface may be according to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, published in May 1998.

9. Document ID: US 6725388 B1

L8: Entry 9 of 15 File: USPT Apr 20, 2004

DOCUMENT-IDENTIFIER: US 6725388 B1
TITLE: Method and system for performing link synchronization between two clock domains by inserting command signals into a data stream transmitted between the two clock domains

Detailed Description Text (11):
Attention now is directed to FIG. 6, an example computer system platform having an example virtual interface expansion bridge (VXB) incorporated therein and utilizing the principles of the present invention. As shown in FIG. 6, the computer system 600 may comprise a processor subsystem 610 (which may be comprised of a plurality of processors and at least one cache memory 612), a memory controller hub (MCH) 620 connected to the processor subsystem 610 (such as by a host or a processor front side bus), a graphics subsystem 630 (possibly including a AGP 4.times.graphics controller, a local memory and a display device such as a cathode ray tube, liquid crystal display, or flat panel display) connected to the memory controller hub 620 by a graphics bus 635 (such as an AGP 2.0 bus), and a memory subsystem 640 storing information and instructions for use by the processor subsystem 610 and having at least one memory element 642 connected to MCH 620 by a memory bus 625. The memory element 642 is preferably a dynamic random-access-memory (DRAM), but may be substituted for read-only-memory (ROM), video random-access-memory (VRAM) and the like. The memory element 642 stores information and instructions for use by the host processors 610a-610n.

10. Document ID: US 6694392 B1

L8: Entry 10 of 15 File: USPT Feb 17, 2004

DOCUMENT-IDENTIFIER: US 6694392 B1

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TITLE: Transaction partitioning

Detailed Description Text (10):
Attention now is directed to FIG. 3, an example computer system platform having an example virtual interface expansion bridge (VXB) incorporated therein according to the principles of the present invention. As shown in FIG. 3, the computer system 300 may comprise a processor subsystem 310 (which may be comprised of a plurality of processors 31a-311n and at least one cache memory 312), a memory controller hub (MCH) 320 connected to the processor subsystem 310 (by a host interface or a front side bus), a graphics subsystem 330 (possibly including a AGP 4.times. graphics controller, a local memory and a display device such as a cathode ray tube, liquid crystal display, or flat panel display) connected to the memory controller hub 320 by a graphics bus (such as an AGP 2.0 bus), and a memory subsystem 340 storing information and instructions for use by the processor subsystem 310 and having at least one memory element 342 connected to MCH 320 by a memory bus. The memory subsystem 340 is preferably a dynamic random-access-memory (DRAM), but may be substituted for read-only-memory (ROM), video random-access-memory (VRAM) and the like.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 11. Document ID: US 6557060 B1

L8: Entry 11 of 15 File: USPT Apr 29, 2003

DOCUMENT-IDENTIFIER: US 6557060 B1
TITLE: Data transfer in host expansion bridge

Detailed Description Text (9):
Attention now is directed to FIG. 3, an example computer system platform having an example virtual interface expansion bridge (VXB) incorporated therein according to the principles of the present invention. As shown in FIG. 3, the computer system 300 may comprise a processor subsystem 310 (which may be comprised of a plurality of processors 311a-311n and at least one cache memory 312), a memory controller hub (MCH) 320 connected to the processor subsystem 310 (such as by a host interface or a front side bus), a graphics subsystem 330 (possibly including a AGP 4.times. graphics controller, a local memory and a display device such as a cathode ray tube, liquid crystal display, or flat panel display) connected to the memory controller hub 320 by a graphics bus 335 (such as an AGP 2.0 bus), and a memory subsystem 340 storing information and instructions for use by the processor subsystem 310 and having at least one memory element 342 connected to MCH 320 by a memory bus 325. The memory subsystem 340 is preferably a dynamic random-access-memory (DRAM), but may be substituted for read-only-memory (ROM), video random-access-memory (VRAM) and the like. The memory subsystem 340 stores information and instructions for use by the host processors 311a-311n.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 12. Document ID: US 6470422 B2

L8: Entry 12 of 15 File: USPT Oct 22, 2002

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DOCUMENT-IDENTIFIER: US 6470422 B2
TITLE: Buffer memory management in a system having multiple execution entities

Detailed Description Text (25):
The main memory 206 is controlled by a memory controller 207 in a memory hub 208 coupled to the CPU 200 over the host bus 203. In addition, the memory hub 208 may include a cache controller 205 operatively coupled to the L2 cache 204. The memory hub 208 may also include a graphics interface 211 that is coupled over a link 209 to a graphics controller 210, which is in turn coupled to a display 212. As an example, the graphics interface may be according to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, published in May 1998.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

13. Document ID: US 6367074 B1

L8: Entry 13 of 15 File: USPT Apr 2, 2002

DOCUMENT-IDENTIFIER: US 6367074 B1
TITLE: Operation of a system

Detailed Description Text (10):
Referring to FIG. 1, in one embodiment, a system 10 includes a central processing unit (CPU) 100, which may include a general-purpose or special-purpose processor such as a microprocessor, microcontroller, an application-specific integrated circuit (ASIC), a programmable gate array (PGA), and the like. The CPU 100 may be coupled over a host bus 103 to a memory hub 108 in one embodiment, which may include a memory controller 107 coupled to a main memory 106. In addition, the memory hub 108 may include a cache controller 105 coupled to an L2 cache 104. The memory hub 108 may also include a graphics interface 111 that is coupled over a link 109 to a graphics controller 110, which is in turn coupled to a display 112. As an example, the graphics interface 111 may be according to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, dated in May 1998.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

14. Document ID: US 6349363 B1

L8: Entry 14 of 15 File: USPT Feb 19, 2002

DOCUMENT-IDENTIFIER: US 6349363 B1
TITLE: Multi-section cache with different attributes for each section

Detailed Description Text (25):
The main memory 206 is controlled by a memory controller 207 in a memory hub 208 coupled to the CPU 200 over the host bus 203. In addition, the memory hub 208 may include a cache controller 205 operatively coupled to the L2 cache 204. The memory

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hub 208 may also include a graphics interface 211 that is coupled over a link 209 to a graphics controller 210, which is in turn coupled to a display 212. As an example, the graphics interface may be according to the Accelerated Graphics Port (A.G.P.) Interface Specification, Revision 2.0, published in May. 1998.

☐ 15. Document ID: US 5786825 A

L8: Entry 15 of 15 File: USPT Jul 28, 1998

DOCUMENT-IDENTIFIER: US 5786825 A
TITLE: Virtual display subsystem in a computer

Detailed Description Text (24):
Reference is now made to FIG. 1 which depicts an exemplary, but not exclusive processing system employing a virtualized display subsystem, practiced in accordance with the principles of the present invention. It is to be understood that while the present invention is described with respect to a highly integrated processing unit, it has general application to all processing systems, including systems having a microprocessor with an external data/address bus with external circuitry attached thereto, such as a memory controller or raster graphics circuitry. However, the preferred embodiment includes a system circuit board 11 (a.k.a. motherboard) preferably having buses to couple together a highly integrated CPU 10 (described in more detail hereinbelow), system memory 36, a RAMDAC/thin film transistor (TFT) interface 40, L2 cache 44, and chipset logic circuitry 49. A multi-tasking operating system program such as Microsoft.RTM. Windows.TM. preferably executes on the CPU 10 to manage primary operations.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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